We Claim:

1. A method of electrochemically filling cavities on a wafer surface to form a substantially planar conductive layer, comprising the steps of:

applying a first cathodic current to form a first conductive layer on the wafer surface, the first conductive layer having a planar portion over a first cavity and a non-planar portion over a second cavity, wherein the first cavity is an unfilled cavity with the smallest width and the second cavity has the next larger width after the smallest cavity, and wherein the first and the second cavities are less than 10 micrometers in width;

treating surface of the first conductive layer by applying a first pulsed current; and

applying a second cathodic current to form a second conductive layer on the first conductive layer, the second conductive layer having a planar portion over both the first and second cavities.

2. The method of claim 1, wherein the step of treating comprises applying an anodic pulsed current as the first pulsed current.

3. The method of claim 1, wherein the step of treating comprises applying a cathodic pulsed current as the first pulsed current.

4. The method of claim 1, wherein the step of treating surface of the first conductive layer prevents bump formation on the surface of the first conductive layer.

5. The method of claim 1, wherein the steps of applying first and second cathodic currents comprise applying a DC voltage.

6. The method of claim 1, wherein the steps of applying first and second cathodic currents comprise applying an AC voltage.

7. The method of claim 11, further comprising the step of repeating the steps of treating and applying until all the cavities on the wafer surface are filled.

8. A semiconductor device manufactured using the method of claim 1.

9. A method to electrochemically fill a plurality of cavities on a wafer surface comprising the steps:

applying a first cathodic current to fill a first cavity and partially fill a second cavity with a first conductive layer on the wafer surface, the first cavity having a smaller width than the second cavity wherein the first cavity and the second cavity each include a width less than 10 micrometers;

applying a pulsed current to treat the first conductive layer; and

applying a second cathodic current to fill the second cavity with a second conductive layer to form a substantially planar conductive layer over the first cavity and the second cavity.

10. The method of claim 9, wherein the step of applying the cathodic current includes a cathodic DC waveform.

11. The method of claim 9, wherein the step of applying the cathodic current includes a cathodic AC waveform.

12. The method of claim 9, wherein the step of applying a pulsed current includes a plurality anodic pulsed current.

13. The method of claim 12, wherein the step of applying the plurality anodic pulsed current includes pulses of approximately 1 second in duration.

14. A semiconductor device manufactured using the method of claim 9.

15. A method of electrochemically filling cavities on a wafer surface to form a substantially planar conductive layer, a first cavity being an unfilled cavity with a smallest width and a second cavity having a next larger width wherein the first and the second cavities are less than 10 micrometers in width, the method comprising:

applying a first cathodic current to form a first conductive layer on the wafer surface, the first conductive layer having a planar portion over a first cavity and a non-planar portion over a second cavity, the first cavity being filled and the second cavity being unfilled;

treating the first conductive layer; and

applying a second cathodic current to form a second conductive layer on the first conductive layer, the second conductive layer having a planar portion over both the first and second cavities.

16. The method of claim 15, wherein the step of applying the cathodic current includes a cathodic rectangular waveform.

17. The method of claim 15, wherein the step of treating includes applying a pulsed current.

18. The method of claim 17, wherein the step of applying a pulsed current includes an anodic current.

19. The method of claim 17, wherein the step of applying a pulsed current includes a cathodic current.

20. The method of claim 15, wherein the planar conductive layer is copper.